HIGH EFFICIENCY S-BAND 30W POWER GaAs FETs

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ABSTRACT

An S-band high-efficiency power GaAs MESFET has been developed by employing the second-harmonic terminating technique in both the input and output matching circuits. This internally matched power FET demonstrates state-of-the-art performance of 30.9W (44.9dBm) output power with more than 60% power-added efficiency and a 15.0 dB linear gain at 2.5GHz. Successful termination of the second-harmonic was confirmed by measuring gate and drain voltage waveforms using EOS (Electro-Optic Sampling). This amplifier can be assembled in a conventional ceramic package, and thus is suitable for satellite communication system applications.

INTRODUCTION

Power amplifiers for mobile communication satellites must meet demands for high efficiency with high output power. In order to achieve high efficiency, harmonic impedance has hitherto been terminated in the output circuits[1]. In a recent investigation, a high efficiency amplifier was achieved by terminating second-harmonic source impedance[2]. However, these source and load harmonic termination technologies have been applied to small-sized power amplifiers of 1W-level. In this work, we aimed to improve efficiency and output power of high-power amplifiers delivering more than 30W by optimally terminating second-harmonic source impedance as well as second-harmonic load impedance. Moreover, in order to confirm successful termination of the second-harmonic, we measured the voltage waveforms of gate and drain electrodes by the contact-less EOS (Electro-Optic Sampling) method[3].

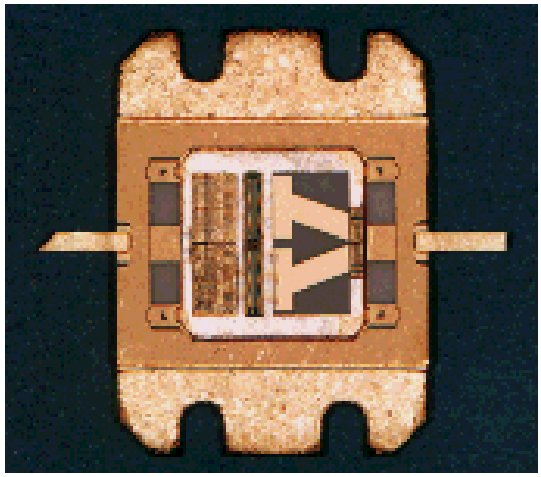

Figure 1. Internal view of the developed amplifier

DEVICE CHARACTERISTICS

We employed power GaAs MESFETs with 1.0 μ m WSi gate fabricated in a step-recessed structure[4]. These devices exhibited typical Idss, Imax, transconductance, threshold voltage and drain breakdown voltage of 200mA/mm, 340mA/mm, 125mS/mm, -2.0V and 25V, respectively.

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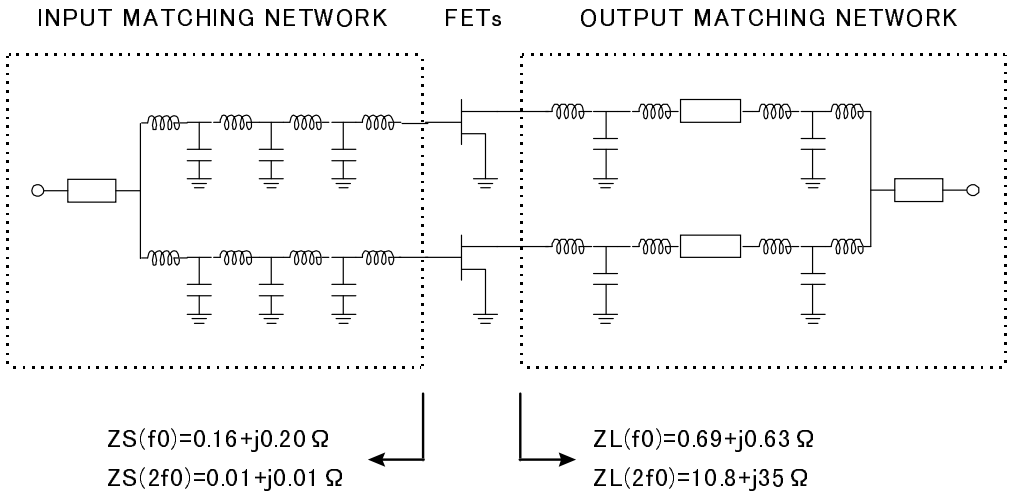


Figure 2. An equivalent circuit of the developed amplifier

AMPLIFIER DESIGN

Figure 1 shows an internal view of the developed amplifier. The amplifier was designed to combine the output power of two FET chips with a total gate width of 86mm. The FET chips were assembled with impedance transforming circuits in a conventional ceramic package. The overall dimension of the amplifier is 24mm × 17.4mm.

Figure 2 shows an equivalent circuit of the developed amplifier. The input internal matching network consists of three stages of a lumped LC low pass filter network. The elements of the input circuit were designed to minimize the loss of matching circuits at the fundamental frequency(2.5GHz) as well as to short the impedance at the second-harmonic frequency(5GHz) on the gate electrode. The optimum source reflection phase at the second-harmonic frequency was experimentally determined to be around short by matching L and C parameters. On the other hand, the output matching network consists of a transmission line and LC low pass filter network. We designed the elements of the output circuit to maximize power-added efficiency at the fundamental frequency. Moreover, we experimentally determined the optimum load phase condition at the second-harmonic frequency by adding one stage of an LC circuit to the drain electrode. The second-harmonic impedance was varied by changing the resonant condition of this additional LC circuit, while the load impedance at the fundamental frequency was kept almost constant by slightly adjusting the other LC circuit elements. Figure 3 shows the dependence of output power and power added efficiency at the 2dB gain compression point on the load phase at the second harmonic frequency. In this way, we experimentally found that the optimum second-harmonic load impedance should be open (phase=0°) rather than short(phase=180°) .

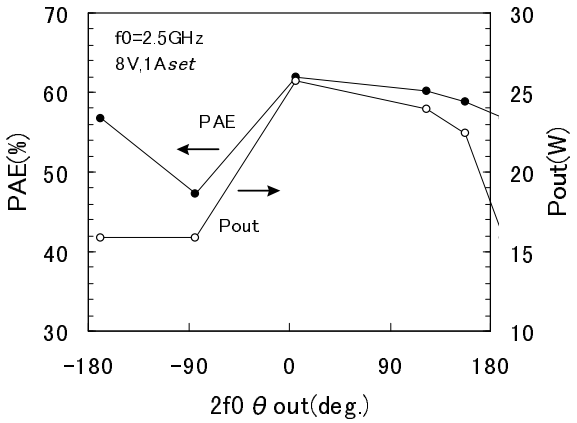


Figure 3. Measured output power and power added efficiency at the 2dB gain compression point versus the load phase at the second-harmonic frequency(5GHz).

AMPLIFIER PERFORMANCE

Measured output power (Pout) and power added efficiency (PAE) versus input power (Pin) are shown in Figure 4. The fabricated amplifier demonstrated an output power of 30.9W (44.9dBm) at the 2dB gain compression point with a 15.0 dB linear gain and 60.5% power-added efficiency with Vd = 8.5V at 2.5GHz. Figure 5 shows the measured output power and power-added efficiency versus drain set-voltage (Vd) at 2.5GHz. At Vd= 9V, it delivered an output power of 35W (45.4Bm) with 59% power-added efficiency. These are the highest efficiencies and output powers at S-band reported so far using power FETs assembled in a conventional ceramic package.

In order to confirm successful termination of the second-harmonic, we measured the voltage waveforms on gate and drain electrodes by the contact-less EOS method. Figure 6 shows gate (marked α) and drain (marked β) voltage waveforms at maximum efficiency operation (Pin=33dBm) measured by EOS for the three amplifiers terminated in different source and load second-harmonic impedances. The amplifier type(A), in which both the source and load second-harmonic impedances are short, delivered Pout of 16W with PAE of 56% at Vd=8V. The drain voltage observed by EOS seems to be a sawtooth waveform. In comparison, the drain voltage of the developed amplifier type(B), in which the source and load second-harmonic impedances are short and open respectively, was found to be a quasi-square waveform. This quasi-square drain voltage with a flat portion at low Vd tends to reduce the overlap of drain-voltage and drain-current in the time domain. This reduction avoids power dissipation and results in PAE improvement. Furthermore, comparing the voltage waveform of the amplifier type(C), in which the source and load second-harmonic impedances are inductive and open respectively, with that of type(B), we see the drain voltage waveform depends significantly on the source second-harmonic phase condition. This indicates the requirement to optimize both the harmonic source and load terminations simultaneously. Among amplifier types (A) to (C), both the gate and drain voltage waves of type(C) seem to be the closest to square waves. However the second-harmonic ripple observed on drain voltage waveform caused power dissipation, resulting in slightly inferior efficiency of type (C) to that of type(B). These results indicate that the developed amplifier type(B) was optimally terminated with respect to the second-harmonic frequency in both source and load matching circuits.

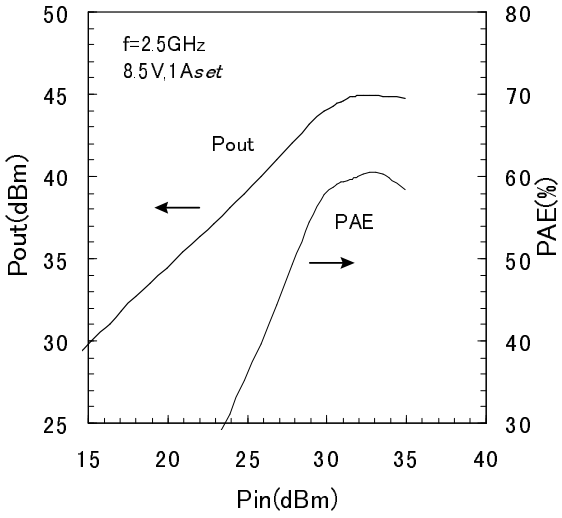


Figure 4. Measured output power and power-added efficiency versus input power at 2.5GHz of the developed amplifier.

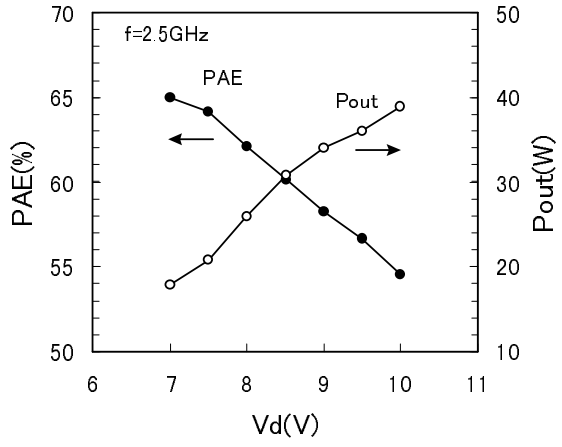


Figure 5. Measured output power and power-added efficiency versus drain set-voltage at 2.5GHz of the developed amplifier.

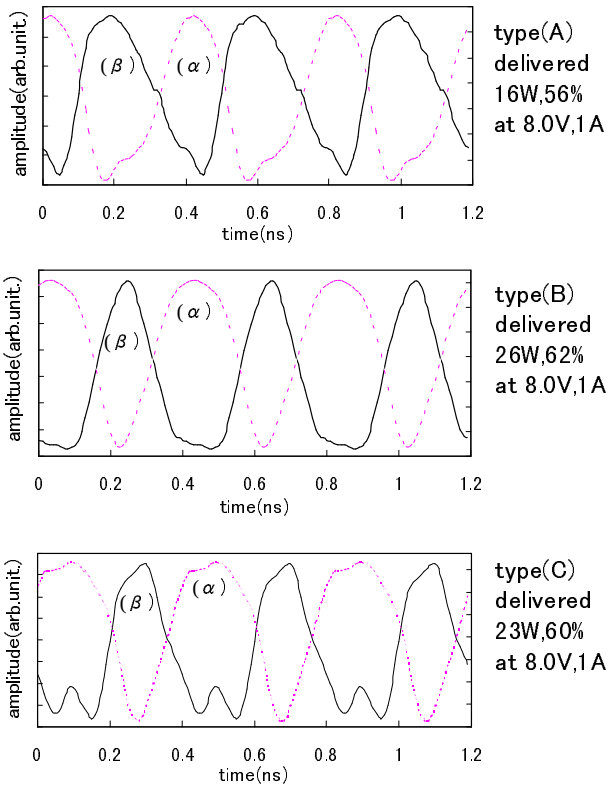
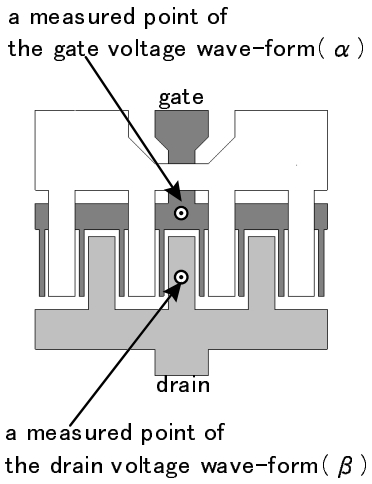


Figure 6. The gate (α) and drain (β) voltage waveform at Pin=33dBm measured by EOS for the three amplifiers.



type	ZS(2f0) Z0=50/32Ω	ZL(2f0) Z0=50/32Ω
(A)	0.01-j0.05(0.98∠186°) short	0.02-j0.1(0.96∠192°) short
(B)	0.01-j0.05(0.98∠186°) short	6.9+j22.3(0.97∠5.2°) open
(C)	0.01+j0.58(0.98∠119°) inductive	6.9+j22.3(0.97∠5.2°) open

CONCLUSION

An S-band high-efficiency power GaAs MESFET has been developed by employing the second-harmonic terminating technique in both the input and output matching circuits. This internally matched power FET demonstrates state-of-the-art performance of 30.9W (44.9dBm) output power with more than 60% power-added efficiency at 2.5GHz. This amplifier can be assembled in a conventional ceramic package, and thus is suitable for satellite communication system applications.

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